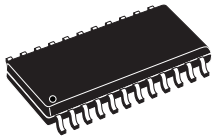
L9823

Octal Low-Side Driver for bulb, resistive and inductive loads with serial input control, output protection and diagnostic

- OUTPUTS CURRENT CAPABILITY UP TO 0.5A
- CASCADABLE SPI CONTROL FOR OUTPUTS
- RESET FUNCTION WITH RESET SIGNAL OR UNDERVOLTAGE AT V_{DD}
- PROGRAMMABLE INTRINSIC OUTPUT VOLTAGE CLAMPING AT TYP. 50V FOR INDUCTIVE SWITCHING
- OVERCURRENT SHUTDOWN WITH LATCH-OFF FOR EVERY WRITE CYCLE (SFPD = LOW)
- INDEPENDENT THERMAL SHUTDOWN OF OUTPUTS (SOA PROTECTION)
- OUTPUT STATUS DATA AVAILABLE ON THE SPI USING 8-BIT I/O PROTOCOL UP TO 3.0MHZ
- LOW STANDBY CURRENT WITH RESET = LOW (TYP 35µA @ VDD)
- OPEN LOAD DETECTION (OUTPUTS OFF)
- SINGLE V_{DD} LOGIC SUPPLY
- HIGH EMS IMMUNITY AND LOW EME (CONTROLLED OUTPUT SLOPES)
- FULL FUNCTIONALITY OF THE REMAINING DEVICE AT NEGATIVE VOLTAGE DROP ON OUTPUTS (-1,5V OR -3,0A)
- OUTPUT MODE PROGRAMMABLE FOR SUSTAINED CURRENT LIMIT OR SHUTDOWN

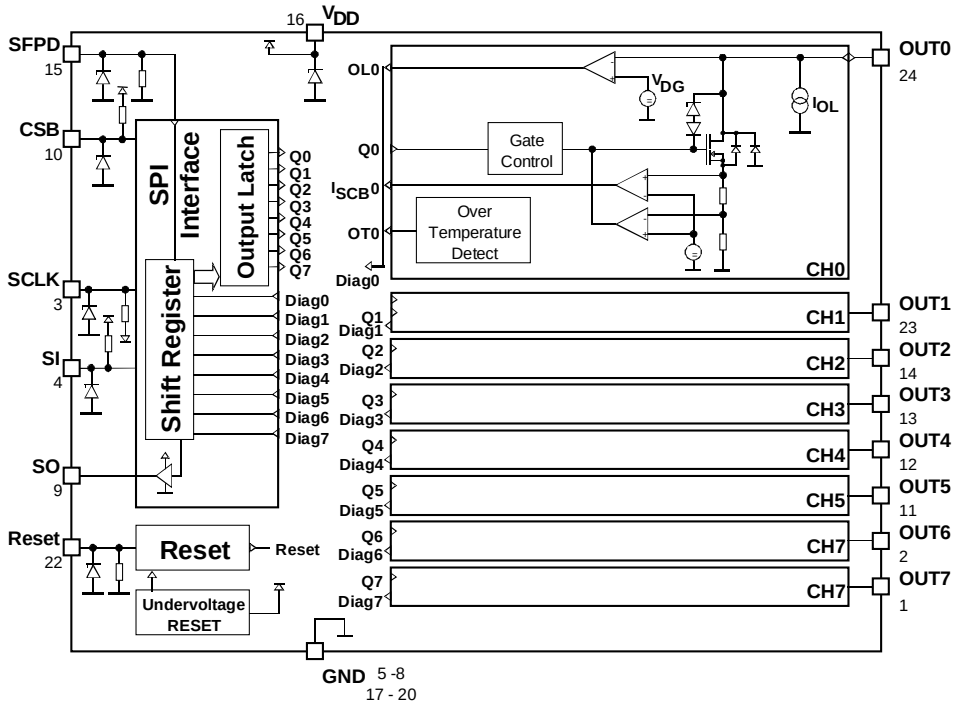


SO24 (20+2+2)
ORDERING NUMBER: L9823

DESCRIPTION

L9823 is a Octal Low-Side Driver Circuit, dedicated for automotive applications. Output voltage clamping is provided for flyback current recirculation, when inductive loads are driven. Chip Select and cascadable Serial 8-bit Interface for outputs control and diagnostic data transfer.

BLOCK DIAGRAM



PIN FUNCTION

N°	Pin	Description
1	Out 7	Output 7
2	Out 6	Output 6
3	SCLK	SCLK. The system clock pin (SCLK) clocks the internal shift registers of the L9823. The serial input pin (SI) accepts data into the input shift register on the falling edge of the SCLK signal while the serial output pin (SO) shifts data information out of the shift register on the rising edge of the SCLK signal. False clocking of the shift register must be avoided to guarantee validity of data. It is essential that the SCLK pin be in a logic low state whenever chip select bar pin (CSB) makes any transition. For this reason, it is recommended though not necessary, that the SCLK pin be kept in a low logic state as long as the device is not accessed (CSB in logic high state). When CSB is in a logic high state, any signal at the SCLK and SI pin is ignored and SO is tri-stated (high-impedance).
4	SI	SI. This pin is for the input of serial instruction data. SI information is read in on the falling edge of SCLK. A logic high state present on this pin when the SCLK signal rises will program a specific output OFF, and in turn, turns OFF the specific output on the rising edge of the CSB signal. Conversely, a logic low state present on the SI pin will program the output ON, and in turn, turns ON the specific output on the rising edge of the CSB signal. To program the eight outputs of the L9823 ON or OFF, an eight bit serial stream of data is required to be entered into the SI pin starting with Output 7, followed by Output 6, Output 5, etc., to Output 0. For each rise of the SCLK signal, with CSB held in a logic low state, a databit instruction (ON or OFF) is loaded into the shift register per the databit SI state. The shift register is full after eight bits of information have been entered. To preserve data integrity, care should be taken to not transition SI as SCLK transitions from a low-to-high logic state.
5	GND	GND
6	GND	GND
7	GND	GND
8	GND	GND
9	SO	SO. The serial output (SO) pin is the tri-stateable output from the shift register. The SO pin remains in a high impedance state until the CSB pin goes to a logic low state. The SO data reports the drain status, either high or low. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. When an output is OFF and not faulted, the corresponding SO databit is a high state. When SO an output is ON, and there is no fault, the corresponding databit on the SO pin will be a low logic state. The SI / SO shifting of data follows a first-in-first-out protocol with both input and output words transferring the Most Significant Bit (MSB) first. The SO pin is not affected by the status of the Reset pin.
10	CSB	CSB. The system MCU selects the L9823 to be communicated with through the use of the CSB pin. Whenever the pin is in a logic low state, data can be transferred from the MCU to the L9823 and vise versa. Clocked-in data from the MCU is transferred from the L9823 shift register and latched into the power outputs on the rising edge of the CSB signal. On the falling edge of the CSB signal, drain status information is transferred from the power outputs and loaded into the device's shift register. The CSB pin also controls the output driver of the serial output pin. Whenever the CSB pin goes to a logic low state, the SO pin output driver is enabled allowing information to be transferred from the L9823 to the MCU. To avoid any spurious data, it is essential that the high-to-low transition of the CSB signal occur only when SCLK is in a logic low state.
11	Out 5	Output 5
12	Out 4	Output 4
13	Out 3	Output 3

PIN FUNCTION (continued)

N°	Pin	Description
14	Out 2	Output 2
15	SFPD	SFPD. The Short Fault Protect Disable (SFPD) pin is used to disable the overcurrent latch-OFF. This feature allows control of incandescent loads where in-rush currents exceed the device's analog current limits. Essentially the SFPD pin determines whether the L9823 output(s) will instantly shutdown upon sensing an output short or remain ON in a current limiting mode of operation until the output short is removed or thermal shutdown is reached. If the SFPD pin is tied to V_{DD} the L9823 output(s) will remain ON in a current limited mode of operation upon encountering a load short to supply. If the SFPD pin is grounded, a short circuit will immediately shutdown only the output affected. Other outputs not having a fault condition will operate normally.
16	VDD	VDD
17	GND	GND
18	GND	GND
19	GND	GND
20	GND	GND
21	NC	Not Connected
22	Reset	Reset. The Reset pin is active low and used to clear the SPI shift register and in doing so sets all output switches OFF. With the device in a system with an MCU; upon initial system power up, the MCU holds the Reset pin of the device in a logic low state ensuring all outputs to be OFF until the VDD pin voltages are adequate for predictable operation. After the L9823 is Reset, the MCU is ready to assert system control with all output switches initially OFF. The Reset pin is active low and has an internal pull-down incorporated to ensure operational predictability should the external pull-down of the MCU open circuit. The internal pull-up is to afford safe and easy interfacing to the MCU. The Reset pin of the L9823 should be pulled to a logic low state for a duration of at least 160ns to ensure reliable Reset.
23	Out 1	Output 1
24	Out 0	Output 0

ABSOLUTE MAXIMUM RATINGS

For voltages and currents applied externally to the device. Exceeding limits may cause damage to the device.

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.3 to 7	V
Inputs and data lines (CSB, SCLK, SI, Reset, SFPD, SO)			
V_{IN}	Voltage (CSB, SCLK, SI, Reset, SFPD)	-0.3 to 7	
V_{SDO}	Voltage (SO)	-0.3 to V_{DD}+0.3	V
I_{IN}	Protection diodes current [1] $T \leq 1ms$	-20 to 20 [1]	mA
Outputs (Out0 ... Out7)			
$V_{OUT\ Cont}$	Continuous output voltage	-1.5 to 45	V

ABSOLUTE MAXIMUM RATINGS (continued)

Symbol	Parameter	Value	Unit
$V_{OUT\ Cont}$	Continuous output current	-3 to $I_{OUT\ LIM}$	A
$I_{OUT\ PEAK}$	Output current	-10 [2] to 2	A
$E_{OUTclamp}$	Output clamp energy [3]	50	mJ
$I_{OUT\ LIM}$	Output current (self limit)	2	A

Note 1) All inputs are protected against ESD according to MIL 883C; tested with HBM C = 100pF, R = 1500Ω at ±2KV. It corresponds to a dissipated energy E ≤ 0.2mJ (data available upon request).
2) Transient pulses in accordance to DIN40839 part 1, 3 and ISO 7637 Part 1, 3.
3) Max. output clamp energy at T_j = 150°C, using single non-repetitive pulse of 500mA

THERMAL DATA

Symbol	Parameter	Value	Unit
Thermal shutdown			
T_{LIM}	Thermal shutdown threshold	155 (Min.), 180 (Typ.)	°C
Thermal resistance (junction-to-Lead)			
$R_{thjL\text{-}one}$	Single output (junction lead)	25 (Max.)	°C/W
$R_{thjL\text{-}all}$	All outputs (junction lead)	20 (Max.)	°C/W
T_{stg}	Storage Temperature	-55 to 150	°C

ELECTRICAL CHARACTERISTCS (4.5V ≤ V_{DD} ≤ 5.5V; -40°C ≤ T_J ≤ 150°C; unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply voltage						
I_{DDSTB} I_{DDleak}	Standby current leakage current	Reset = LOW and / or V_{DDRES}>V_{DD} > 0.5V V_{DD} < 0.5V		35 <1	70 10	µA µA
I_{DDOPM}	Operating mode	$I_{OUT0\ ...\ 7}$ = 500mA SPI - SCLK = 3MHz CSB = LOW SO no load			6	mA
$\Delta I_{DD\ rev}$	ΔI_{DD} during reverse output current	$I_{out\ rev}$ = -2.5A			10	mA
$V_{DD\ RES}$	Undervoltage Reset	Reset of all registers and disable of all outputs	2.5		3.95	V
Inputs (CSB, SCLK, SI, Reset, SFPD)						
V_{INL}	Low level		-0.3		0.2·V_{DD}	V
V_{INH}	High level		0.7·V_{DD}		V_{DD}+0.3	V
V_{hyst}	Hysteresis voltage		0.5	1.2	0.5·V_{DD}	V

ELECTRICAL CHARACTERISTCS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{IN}	Input current	$V_{IN} = V_{DD}$	-10		10	µA
R_{IN}	Pullup resistance (CSB, SI) Pulldown resistance (SFPD, Reset, SCLK)		50		250	kΩ
C_{IN}	Input capacitance				10	pF
Serial data outputs						
V_{SOH}	High output level	I_{SO} = -4mA	V_{DD} -0.4			V
V_{SOL}	Low output level	I_{SO} = 3,2mA			0.4	V
I_{SOL}	Tristate leakage current	CSB = high; $0V \le V_{SO} \le V_{DD}$	-10		10	µA
C_{SO}	Output capacitance	f_{SO} = 300kHz, $0V \le V_{SO} \le V_{DD}$			20	pF
Outputs OUT 0 ... 7						
$I_{OUTL0 - 7}$	Leakage current	OUTx = OFF; V_{OUTx} = 16V; $V_{DD} \le V_{DD\ RES}$ and / or Reset = Low Tj ≤ 85°C	-10	<1µA	10	µA
$V_{OUT\ clamp}$	Output clamp voltage	$2mA \le I_{OUT\ clamp} \le I_{OUT\ LIM}$ $I_{OUT\ test}$ = 20mA with correlation	45		60	V
R_{DSon}	On resistance OUT 0 ... 7	I_{OUT} = 500mA;T_j = +150°C T_j = +25°C		1 0.8	1.5 1.25	Ω Ω
C_{OUT}	Output capacitance	V_{OUT} = 16V; f = 1MHz			300	pF
Outputs short circuit protection						
I_{SCB}	Overcurrent shutoff threshold	SFPD = Low, $V_{OUT} \ge V_{DG}$	0.5	1.6	2.5	A
$I_{OUT\ LIM}$	Short circuit current limitation		0.5	1.6	2.5	A
$t_{dly\ SCB}$	Short circuit shutdown delay	SFPD = Low, $V_{OUT} \ge V_{DG}$ CSB = 50% to $I_{OUT} \le 1/2\ I_{OUT\ LIM}$	70	150	250	µs
Diagnostics						
V_{DG}	Diagnostic threshold voltage		$0.5 \cdot V_{DD}$	$0.55 \cdot V_{DD}$	$0.6 \cdot V_{DD}$	V
$I_{OUT\ OL}$	Open load detection sink current	$V_{out} = V_{DG}$ Output programmed OFF	30	60	100	µA
$t_{dly\ SFPD}$	Diagnostic detection filter time	SFPD = Low, $V_{OUT} \ge V_{DG}$ CSB = 50% to valid data at SO	70	150	250	µs
Outputs timing						
t_{don}	Turn ON delay	CSB = 50% to $R_L = 50\Omega$ $V_{OUT} = 0,9V_{bat}$, V_{bat} = 16V			20	µs

ELECTRICAL CHARACTERISTCS (continued)

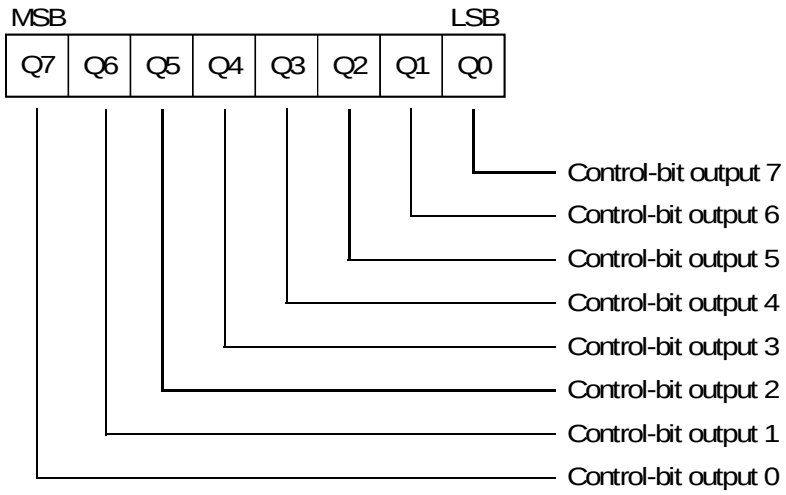
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{doff}	Turn OFF delay	CSB = 50% to R_L = 50Ω V_{OUT} = 0,1·V_{bat}, V_{bat} = 16V			20	µs
$dV_{on/dt}$	Turn ON voltage slew-rate	90% to 30% of V_{bat}; R_L = 50Ω; V_{bat} = 16V	0.7	2.1	3.5	V/µs
$dV_{off/dt}$	Turn OFF voltage slew-rate	30% to 90% of V_{bat}; R_L = 50Ω; V_{bat} = 16V	0.7	2.1	3.5	V/µs
$dV_{off\ clamp/dt}$	Turn OFF voltage clamp slew-rate	30% to 80% of $V_{OUT\ clamp}$ R_L = 500Ω	0.7	2.1	5.5	V/µs
Serial diagnostic link (Load capacitor at SO = 200pF)						
f_{sclk}	Clock frequency	50% duty cycle	3			MHz
t_{clh}	Minimum time SCLK = HIGH		160			ns
t_{cll}	Minimum time SCLK = LOW		160			ns
t_{pcld}	Propagation delay SCLK to data at SO valid	4.9V ≤ V_{DD} ≤ 5.1V			100	ns
t_{csdv}	CSB = LOW to data at SO active				100	ns
t_{sclch}	SCLK low before CSB low	Setup time SCLK to CSB change H/L	100			ns
t_{hclcl}	SCLK change L/H after CSB = Low	Setup time CSB to SCLK change L/H	100			ns
t_{scld}	SI input setup time	SCLK change H/L after SI data valid	20			ns
t_{hcld}	SI input hold time	SI data hold after SCLK change H/L			20	ns
t_{sclcl}	SCLK low before CSB high		150			ns
t_{hclch}	SCLK high after CSB high		15,			ns
t_{pchdz}	CSB L/H to output data float				100	ns
t_{Reset}	Minimum Reset time Reset = Low				160	ns

Outputs Control Tables :

Outputs:

SI-bit	0	1
Output	on	off

Output Control register structure :



Power outputs characteristics

for flyback current, outputs short circuit protection and diagnostics

For output currents flowing into the circuit the output voltages are limited. The typical value of this voltage is 50V. This function allows that the flyback current of a inductive load recirculates into the circuit; the flyback energy is absorbed in the chip.

Output short circuit protection SFPD = Low (dedicated for loads without inrush current): when the output current exceeds the short circuit threshold, the corresponding output overload latch is set after a delay time $t_{dly\ SCB}$ and the output is switched off. The delay timer is started after each rise of CSB and valid datas are transfered to the output control register. If the short takes place after the delay time has elapsed the shutdown is immediate (within 15µs).

Output short circuit protection SFPD = High (dedicated for loads with inrush current, as lamps): when the load current would exceed the short circuit limit value, the corresponding output goes in a current regulation mode. The output current is determined by the output characteristics and the output voltage depends on the load resistance. In this mode high power is dissipated in the output transistor and its temperature increases rapidly. When the power transistor temperature exceeds the thermal shutdown threshold, the overload latch is set and the corresponding output switched off.

For the load diagnostic in output off condition each output features a diagnostic current sink, of typ 60µA.

FUNCTIONAL DESCRIPTION

General

The L9823 integrated circuit features 8 power low-side-driver outputs. Data is transmitted to the device using the Serial Peripheral Interface = SPI protocol. The power outputs features voltage clamping function for flyback current recirculation and are protected against short circuit to Vbat.

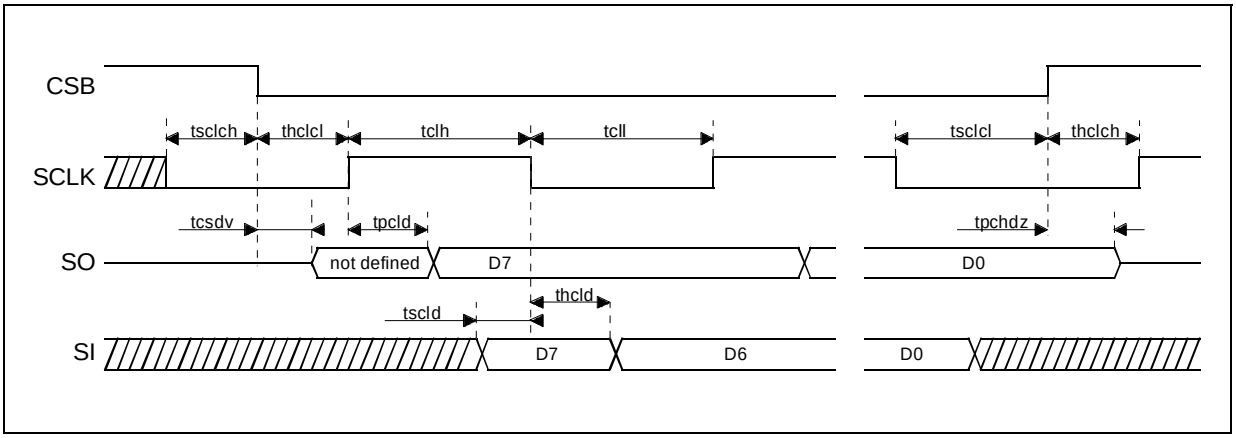
The diagnostics recognizes two outputs fault conditions: 1) overcurrent and thermal overload in switch-ON condition and 2) open load or short to GND in switch-OFF condition for all outputs. The outputs status can be read out via the serial interface.

The chip internal Reset is a OR function of the external Reset signal and internally generated undervoltage Reset signal.

Output Stages Control

Each output is controlled with its latch and with a common Reset line, which enables all outputs.
The control data are transmitted via the SI input, the timing of the serial interface is shown in Fig. 1.
The device is selected with low CSB signal and the input data are transferred into the 8 bit shift register at every falling SCLK edge. The rising edge of the CSB latches the new data from the shift register to the drivers.

Figure 1. Timing of the Serial Interface



The SPI register data are transferred to the output latch at rising CSB edge. The digital filter between CSB and the output latch ensures that the data are transferred only after 8 SCLK cycles or multiple of 8 SCLK cycles since the last CSB falling edge. The CSB changes only at low SCLK.

Diagnostics

The output voltage at all outputs is compared with the diagnostic threshold, typ 0,55 • V_{DD} = V_{DG}.
Diagnostic Table for outputs:

Output	Output-voltage	Status-bit	Output-mode
off	> DG-threshold	high	correct operation
off	< DG-threshold	low	fault condition 2)
on	< DG-threshold	low	correct operation
on	> DG-threshold	high	fault condition 1)

Fault condition 1) "output short circuit to Vbat" : For SFPD = Low the output was switched on and the voltage at the output exceeded the diagnostics threshold due to overcurrent, the output overload latch was set and the output has been switched off. The diagnostic bit is high.
: For SFPD = High the output was switched on and the voltage at the output exceeds the diagnostics threshold. The output operates in current regulation mode or has been switched off due to thermal shutdown. The status bit is high.
Fault condition 2) "open load" or "output short circuit to GND" : the output is switched off and the voltage at the output drops below the diagnostics threshold, because the load current is lower than the output diagnostic current source, the load is interrupted. The diagnostic bit is low.
At the falling edge of CSB the output status data are transferred to the shift register. When SCB is low, data bits contained in the shift register are transferred to SO output at every rising SCLK edge.

Figure 2. Pulse Diagram to Read the Outputs Status Register

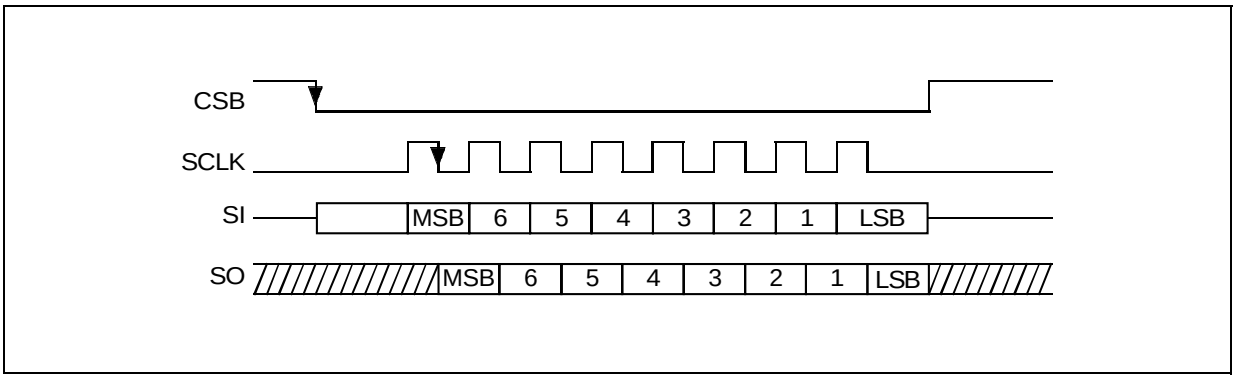
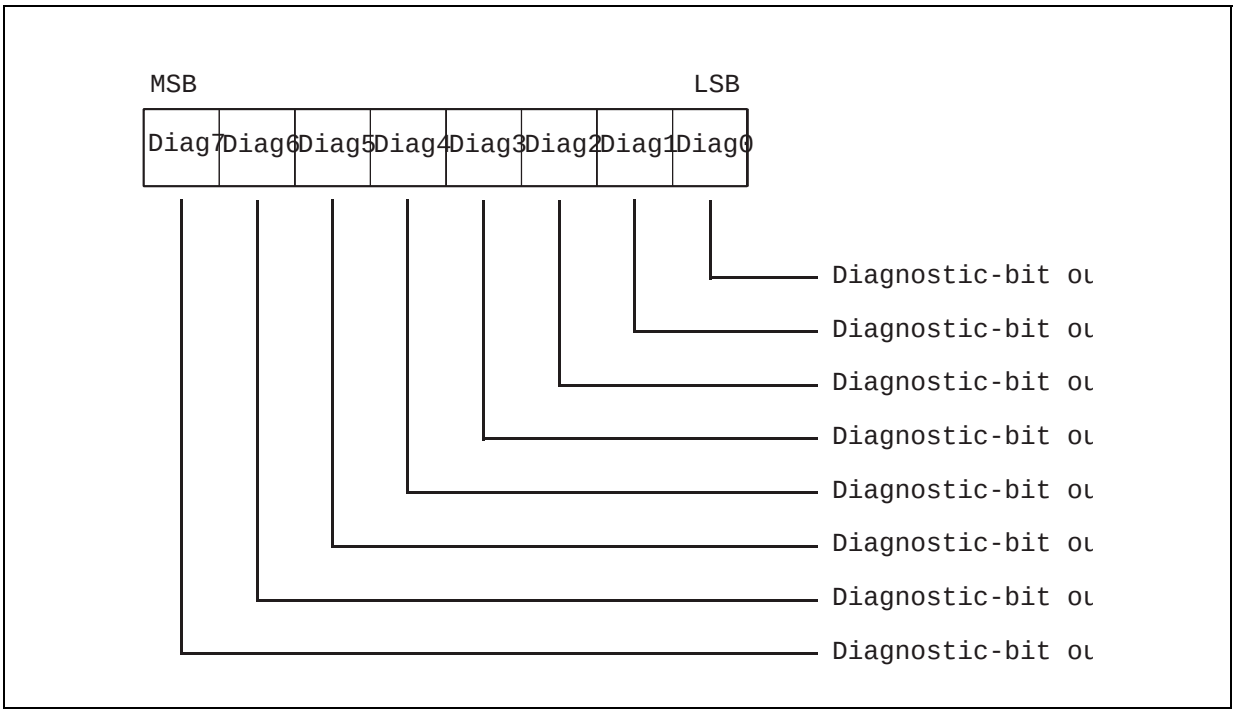


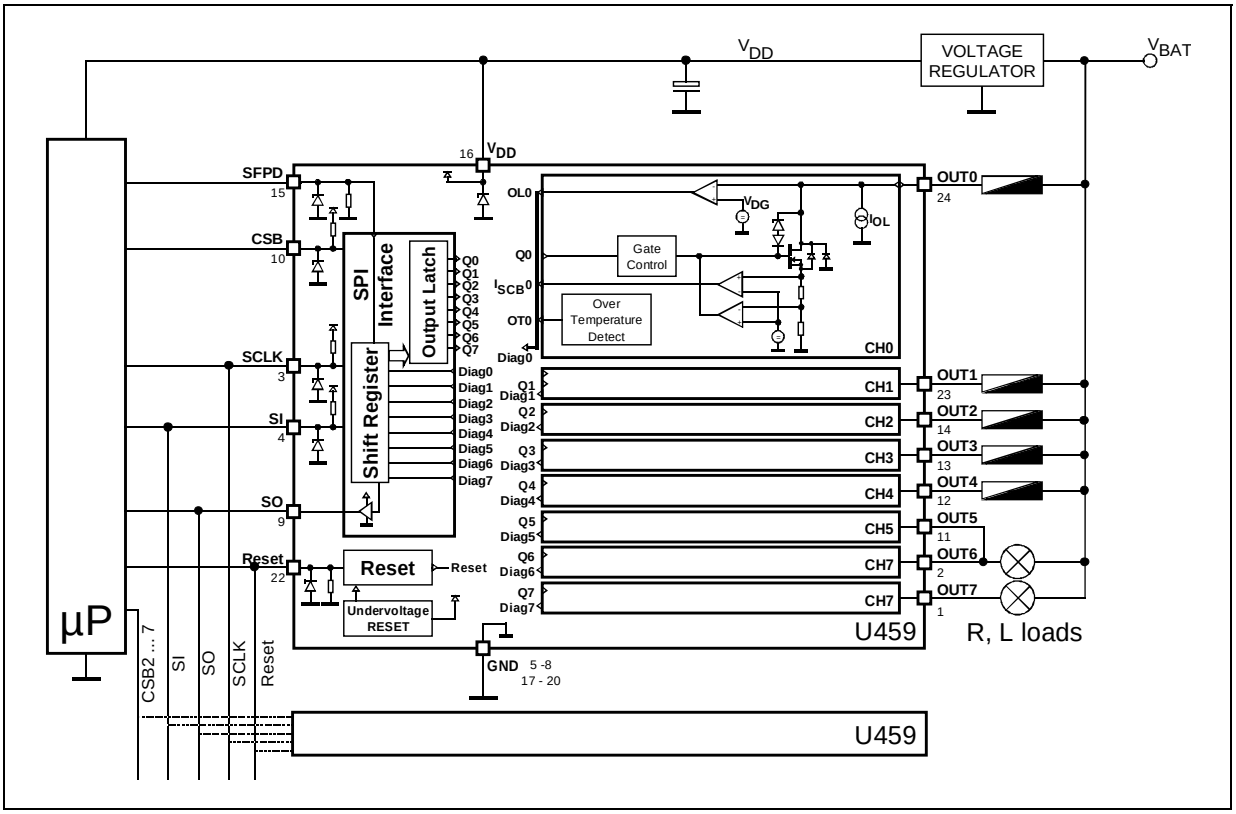
Figure 3. Structure of the Outputs Status Register



APPLICATIONS INFORMATION

The typical application diagram for parallel Input SPI control is shown in Figure 4.

Figure 4. Typical Application Circuit Diagram for the L9823 Circuit.



For higher current driving capability more outputs of the same kind can be paralleled. In this case the maximum flyback energy should not exceed the limit value for single output.

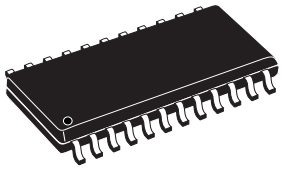
The immunity of the circuit with respect to the transients at the output is verified during the characterization for Test Pulses 1, 2 and 3a, 3b, DIN40839 or ISO7637 part 3. The Test Pulses are coupled to the outputs with 200pF series capacitor. The correct function of the circuit with the Test Pulses coupled to the outputs is verified during the characterization for the typical application with R = 16Ω to 200Ω, L= 0 to 600mH loads. All outputs withstand testpulses without damage.

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	15.20		15.60	0.598		0.614
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0;75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA

Weight: 0.60gr



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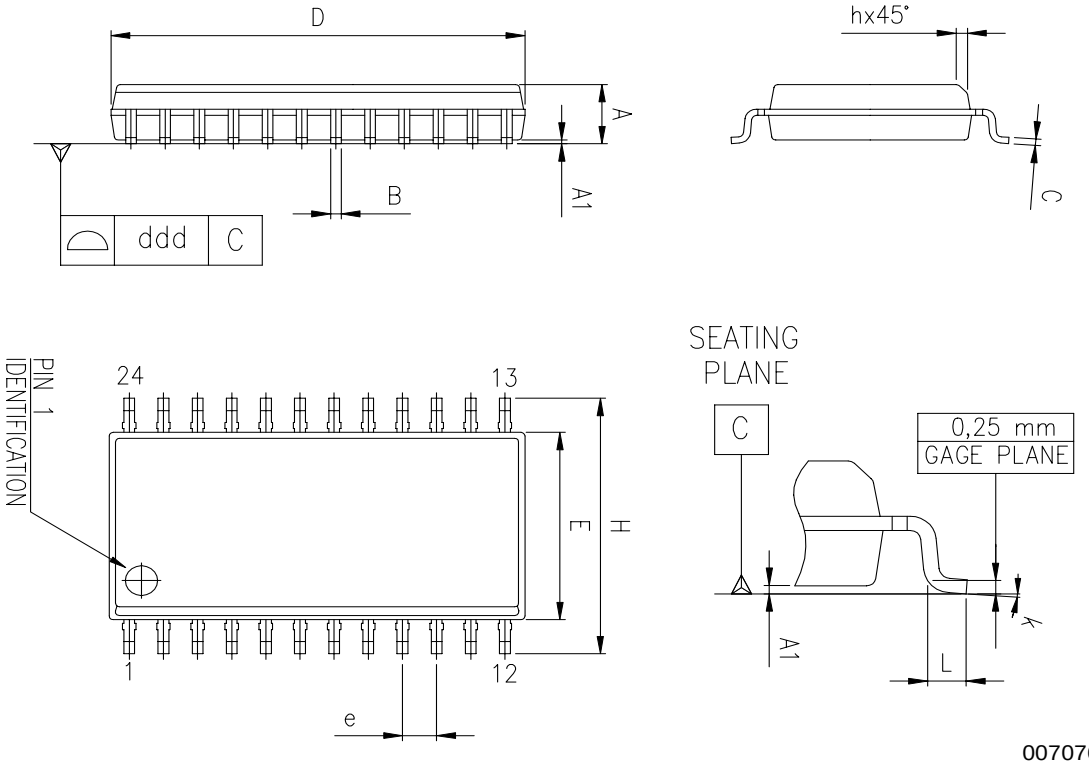

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