

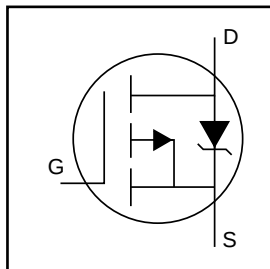


KERSEMI

IRF4905S/L

HEXFET® Power MOSFET

- Advanced Process Technology
- Surface Mount (IRF4905S)
- Low-profile through-hole (IRF4905L)
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated



$$V_{DS} = -55V$$

$$R_{DS(on)} = 0.02\Omega$$

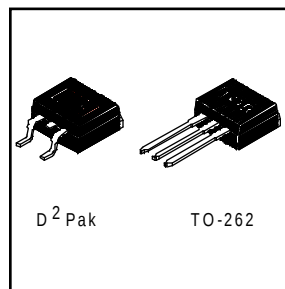
$$I_D = -74A$$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF4905L) is available for low-profile applications.



D² Pak

TO-262

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, V_{GS} @ -10V ^⑤	-74	A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, V_{GS} @ -10V ^⑤	-52	
I_{DM}	Pulsed Drain Current ^{①⑤}	-260	
P_D @ $T_A = 25^\circ C$	Power Dissipation	3.8	W
P_D @ $T_C = 25^\circ C$	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ^{②⑤}	930	mJ
I_{AR}	Avalanche Current ^①	-38	A
E_{AR}	Repetitive Avalanche Energy ^①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ^{③⑤}	-5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

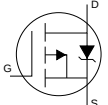
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted,steady-state)**	—	40	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	—	—	V	$V_{GS} = 0V$, $I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.05	—	V/°C	Reference to 25°C , $I_D = -1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.02	Ω	$V_{GS} = -10V$, $I_D = -38A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
g_{fs}	Forward Transconductance	21	—	—	S	$V_{DS} = -25V$, $I_D = -38A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	$V_{DS} = -55V$, $V_{GS} = 0V$
		—	—	-250		$V_{DS} = -44V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	180	nC	$I_D = -38A$
Q_{gs}	Gate-to-Source Charge	—	—	32		$V_{DS} = -44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	86		$V_{GS} = -10V$, See Fig. 6 and 13 ④ ⑤
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = -28V$
t_r	Rise Time	—	99	—		$I_D = -38A$
$t_{d(off)}$	Turn-Off Delay Time	—	61	—		$R_G = 2.5\Omega$
t_f	Fall Time	—	96	—		$R_D = 0.72\Omega$, See Fig. 10 ④
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	3400	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1400	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	640	—		$f = 1.0MHz$, See Fig. 5 ⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-74	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-260		
V_{SD}	Diode Forward Voltage	—	—	-1.6	V	$T_J = 25^\circ\text{C}$, $I_S = -38A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	89	130	ns	$T_J = 25^\circ\text{C}$, $I_F = -38A$
Q_{rr}	Reverse Recovery Charge	—	230	350	nC	$di/dt = -100A/\mu s$ ④ ⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 1.3mH$
 $R_G = 25\Omega$, $I_{AS} = -38A$. (See Figure 12)
- ③ $I_{SD} \leq -38A$, $di/dt \leq -270A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

- ⑤ Uses IRF4905 data and test conditions

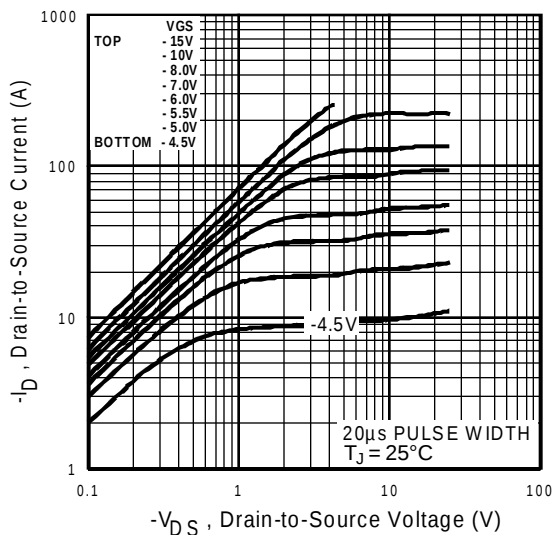


Fig 1. Typical Output Characteristics

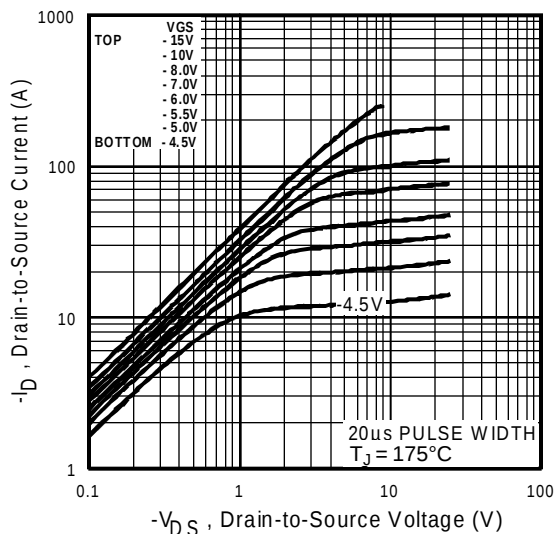


Fig 2. Typical Output Characteristics

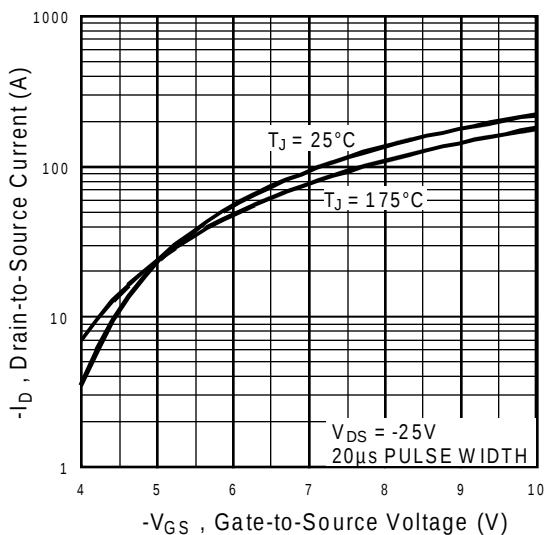


Fig 3. Typical Transfer Characteristics

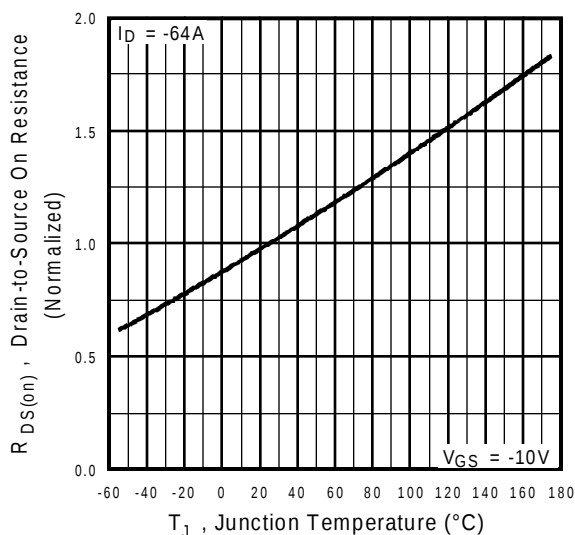
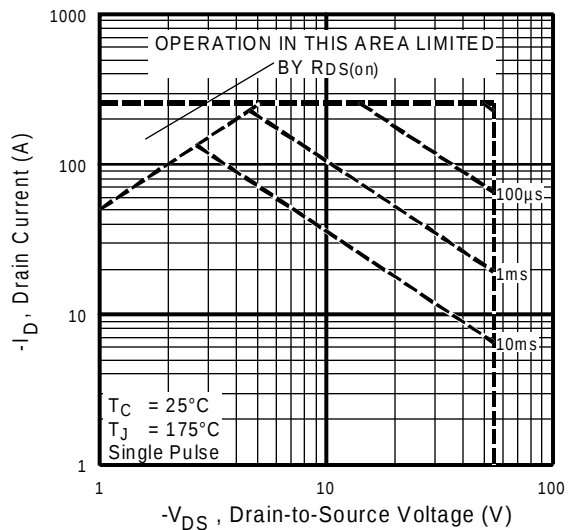
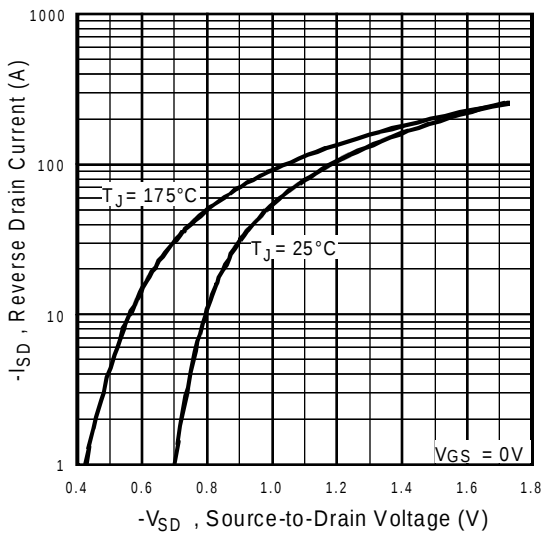
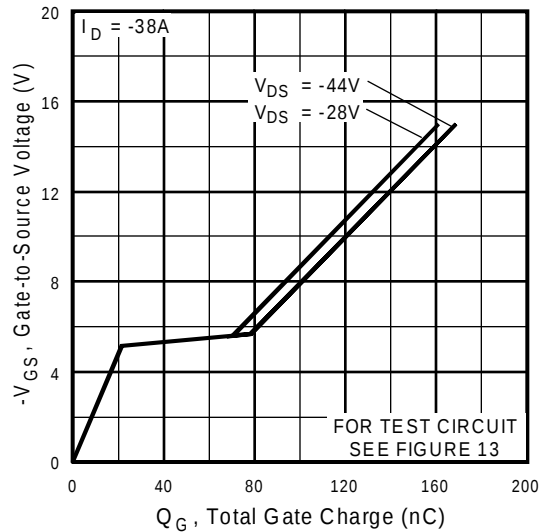
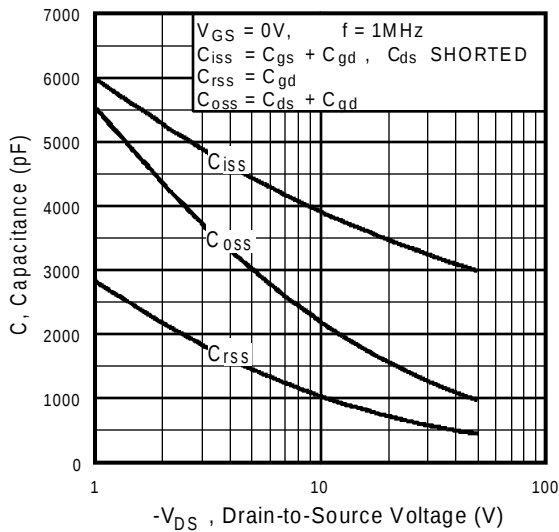


Fig 4. Normalized On-Resistance Vs. Temperature

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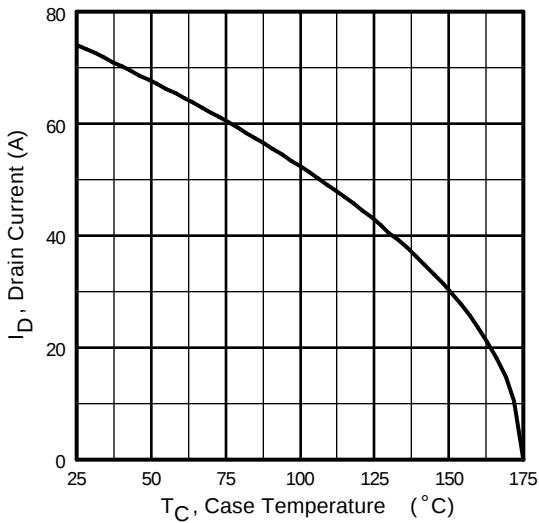


Fig 9. Maximum Drain Current vs. Case Temperature

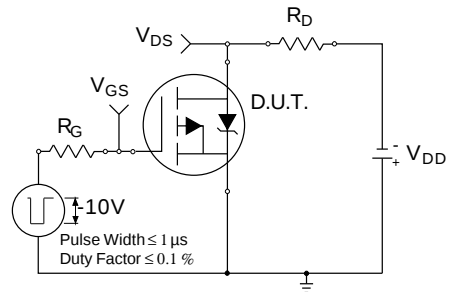


Fig 10a. Switching Time Test Circuit

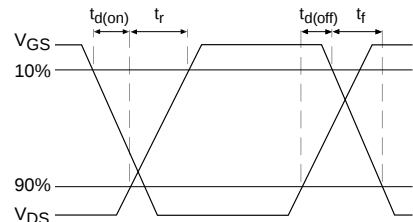


Fig 10b. Switching Time Waveforms

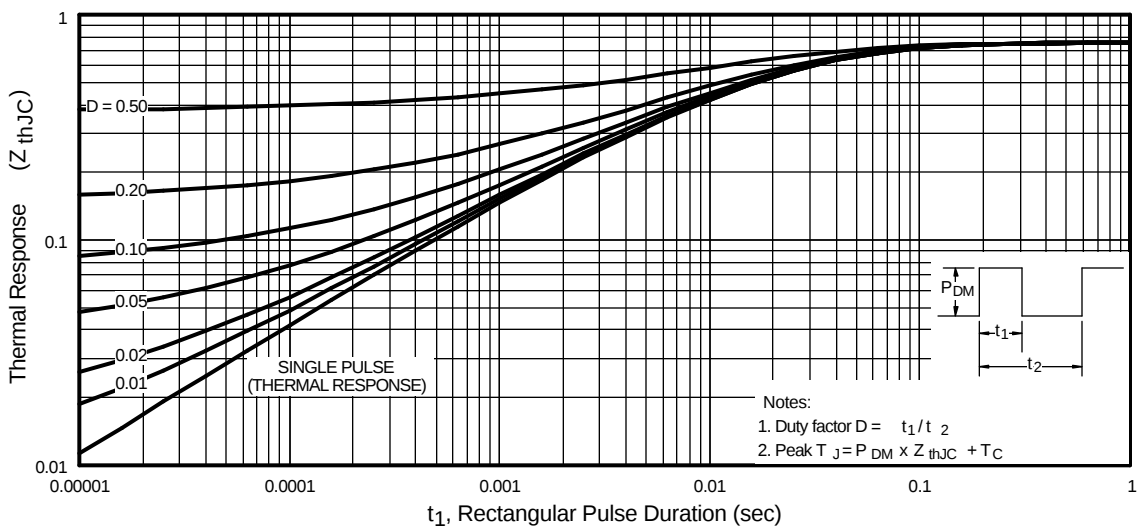


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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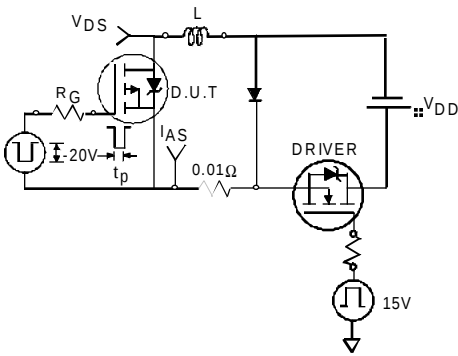


Fig 12a. Unclamped Inductive Test Circuit

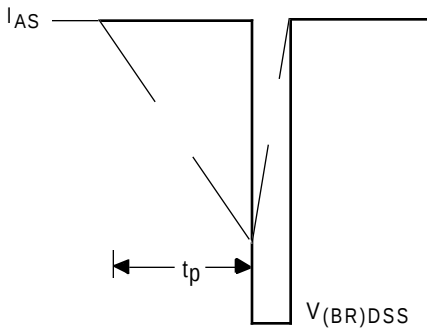


Fig 12b. Unclamped Inductive Waveforms

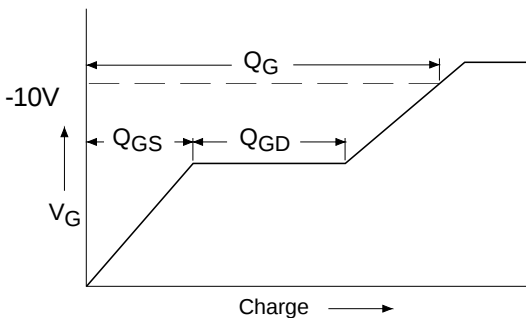


Fig 13a. Basic Gate Charge Waveform

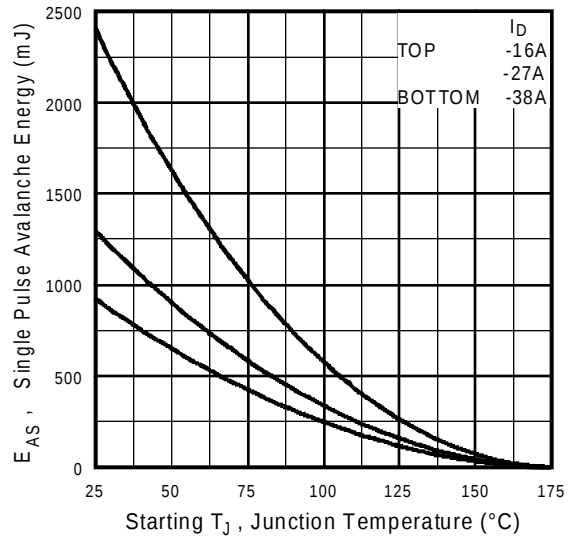


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

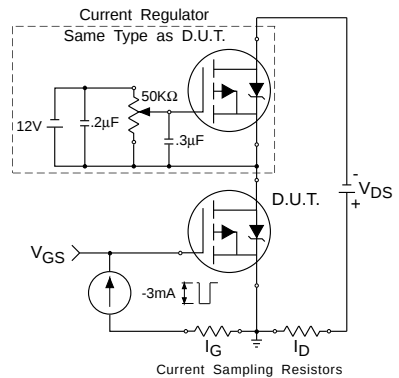
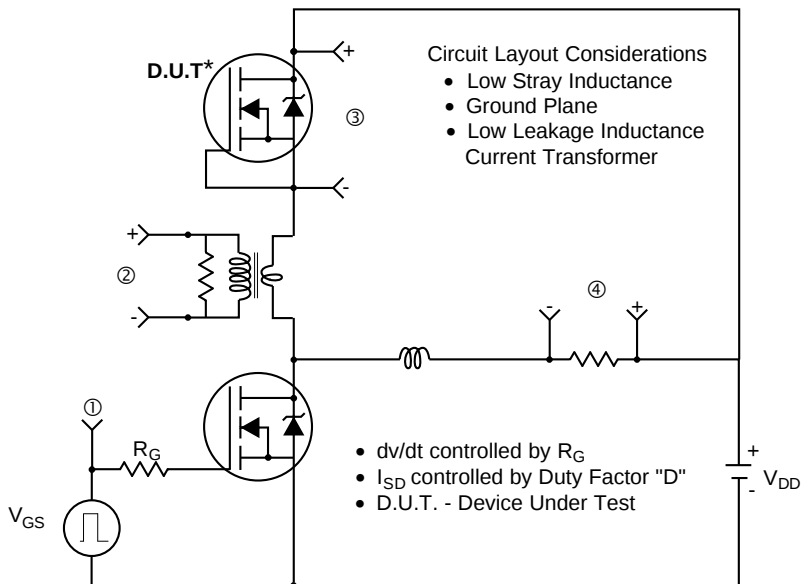
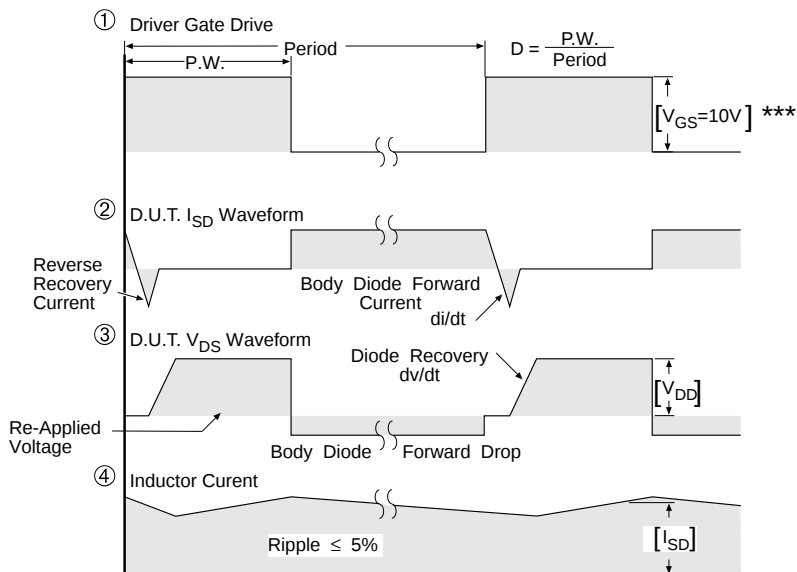


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



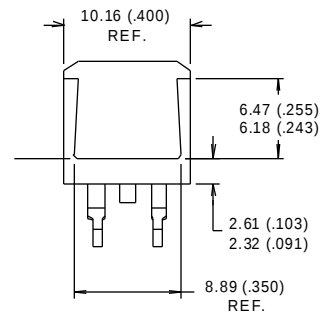
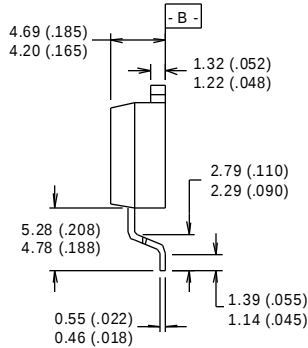
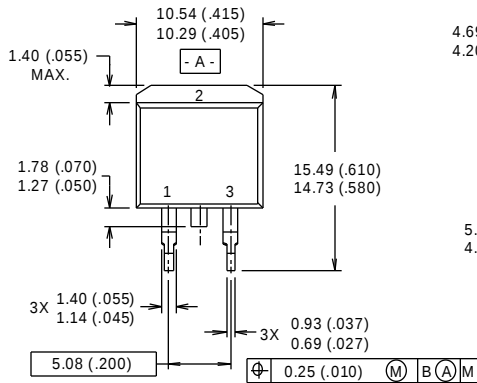
* Reverse Polarity of D.U.T for P-Channel



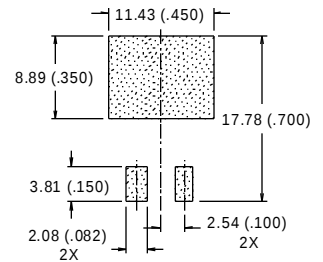
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

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MINIMUM RECOMMENDED FOOTPRINT



NOTES:

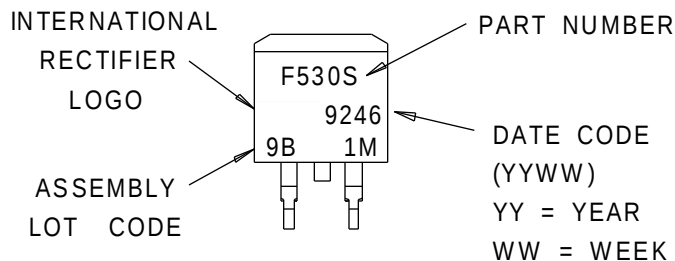
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

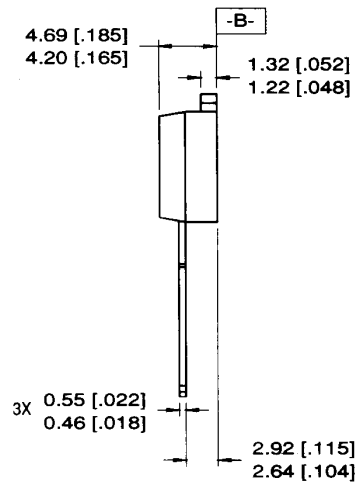
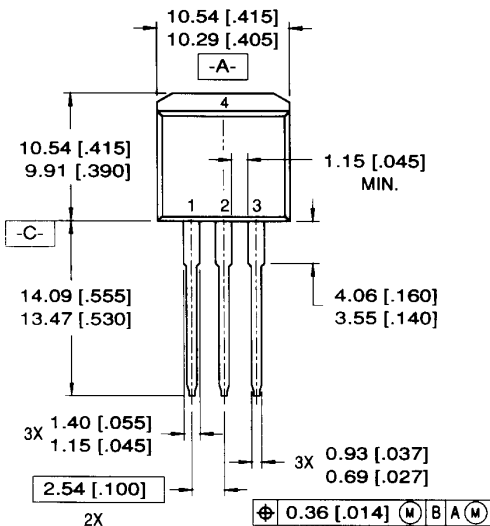
Part Marking Information

D²Pak



Package Outline

TO-262 Outline



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

Part Marking Information

TO-262

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"

